ABSTRACT OF THE DISCLOSURE

In a clock extracting circuit according to the present invention, after serial data is subjected to oversampling using a reference clock of 2N times a frequency of the serial data, clock timing in a period of time in which signal level remains unchanged for a long duration is extracted by first timing detecting means. Clock timing based on a point of change in the signal level is extracted by second timing detecting means, and a final clock timing signal is outputted according to these timings detected. Thus, clock timing can be extracted accurately without omission even when the input signal includes jitter. Further, the clock extraction is performed without converting the input signal into parallel data and by simple processing. A clock extracting circuit for extracting a clock signal from the received serial data with high accuracy is thus realized without increasing the circuit scale.